REMARKS

Claims 1, 4-10, and 13-32 are pending in this application. The present Amendment amends claims 1, 4, 8, 10, 13, 17, 19, and 26, and cancels claims 2, 3, 11, and 12 without prejudice. Claims 5-7, 9, 14-16, 18, 20-25, and 27-32 remain unchanged. Support for the amendments is discussed below. No new matter has been introduced. Favorable reconsideration of the application in light of the foregoing amendments and following comments is respectfully solicited.

Proper Support for Written Description and Enablement Under 35 U.S.C. § 112

On pages 2-4 of the Office Action, claims 1-32 were rejected under 35 U.S.C. 112 as failing to comply with the written description requirement and the enablement requirement. Applicants respectfully traverse.

The original disclosure of the application properly supports the amended claims to satisfy both the written description requirement and enablement requirement under 35 U.S.C. § 112. The Office Action rejected claims 1-32 under § 112, specifically alleging that the original disclosure lacked support for the claimed limitation of "independently selectable" fields used in masked write or bitwise insertion operations. *See* Office Action, p. 2, last paragraph through p. 3, second paragraph. The claim language relating to this limitation is now amended. In the discussion that follows, Applicants set forth (1) the amended claim language relating to "independently selectable" (2) the detailed support found in the disclosure for the amended claim language, and (3) how the support found in the disclosure meets the written disclosure requirement, (4) how the support found in the disclosure meets the enablement requirement.

Amended Claim Language

Amended claims 1 and 10 each recite, *inter alia*:

> . . . the mask consisting of N independently selectable mask bits, N being an integer multiple of eight, each of the mask bits corresponding to a data bit contained in the at least one register, each of the mask bits being independently selectable as either a write-enabled mask bit or a write-disabled mask bit, the execution unit is operable to:
>
> (i) detect some of the mask bits of the mask as being selected as write-enabled mask bits to identify corresponding data bits of the data contained in the at least one register as write-enabled data bits; and
>
> (ii) cause the write-enabled data bits to be written to a specified memory location (*emphasis added*).

Amended claims 19 and 26 each recite, *inter alia*:

> the second operand consisting of N independently selectable bits, N being an integer multiple of eight, wherein each bit in the second operand is independently selectable as either having a first predetermined value or a second predetermined value, wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has the first predetermined value (*emphasis added*).

Support for Amended Claim Language

The original disclosure of the application provides detailed support for the amended claim language relating to the "independently selectable" limitation. The original disclosure includes U.S. Patent Application No. 08/516,036, filed August 16, 1995, which issued as U.S. Patent No. 5,742,840 ("the '840 patent"). The chain of priority linking the original disclosure to the present application includes a continuation-in-part application, U.S. Patent Application No. 09/382,402, which issued as U.S. Patent No. 6,295,599 ("the '599 patent"). The '840 and '599 disclosures each include an appendix submitted as part of the application-as-filed. Both the '840 appendix and the '599 appendix describe instructions that represent illustrative embodiments of instructions that performs a masked write operation or bitwise insertion operation as recited in the claims.

Just as an example, the '840 appendix and '599 appendix each describe the "S.MUX.64.B.A.I" (Store multiplex octlet big-endian aligned immediate) instruction.[1] *See* '840 appendix at pp. 150-157, and the '599 appendix at pp. 123-125 and 128-130. A listing of the "S.MUX.64.B.A.I" instruction from p. 154 of the '840 appendix is reproduced below (highlighting added):

Operation codes

S.8.I[47]	Store byte immediate
S.16.B.A.I	Store double big-endian aligned immediate
S.16.B.I	Store double big-endian immediate
S.16.L.A.I	Store double little-endian aligned immediate
S.16.L.I	Store double little-endian immediate
S.32.B.A.I	Store quadlet big-endian aligned immediate
S.32.B.I	Store quadlet big-endian immediate
S.32.L.A.I	Store quadlet little-endian aligned immediate
S.32.L.I	Store quadlet little-endian immediate
S.64.B.A.I	Store octlet big-endian aligned immediate
S.64.B.I	Store octlet big-endian immediate
S.64.L.A.I	Store octlet little-endian aligned immediate
S.64.L.I	Store octlet little-endian immediate
S.128.B.A.I	Store hexlet big-endian aligned immediate
S.128.B.I	Store hexlet big-endian immediate
S.128.L.A.I	Store hexlet little-endian aligned immediate
S.128.L.I	Store hexlet little-endian immediate
S.AAS.64.B.A.I	Store add-and-swap octlet big-endian aligned immediate
S.AAS.64.L.A.I	Store add-and-swap octlet little-endian aligned immediate
S.CAS.64.B.A.I	Store compare-and-swap octlet big-endian aligned immediate
S.CAS.64.L.A.I	Store compare-and-swap octlet little-endian aligned immediate
S.MAS.64.B.A.I	Store multiplex-and-swap octlet big-endian aligned immediate
S.MAS.64.L.A.I	Store multiplex-and-swap octlet little-endian aligned immediate
S.MUX.64.B.A.I	Store multiplex octlet big-endian aligned immediate
S.MUX.64.L.A.I	Store multiplex octlet little-endian aligned immediate

The "S.MUX.64.B.A.I" instruction performs a masked write operation or bitwise insertion operation in the manner claimed. The operands of this instruction include the contents of the "ra" register (base address), the contents of the "rb" register pair (mask in the even register of the pair and data in the odd register of the pair), and an immediate value (address offset). The instruction obtains a mask consisting of N independently selectable mask bits from the even register of the "rb" register pair. Here, N is equal to 64 (N = 64), which is a multiple of eight. Each of the 64 mask bits can be independently selected as either a write-enabled mask bit (*e.g.*, "1") or a write-disabled mask bit (*e.g.*, "0"). Each of the 64 mask bits corresponds to a data bit

[1] Other such examples include S.MUX.64.L.A.I (Store multiplex octlet little-endian aligned immediate), S.MUX.64.B.A (Store multiplex octlet big-endian aligned), and S.MUX.64.L.A (Store multiplex octlet little-endian aligned).

contained in the odd register of the "rb" register pair The write-enabled mask bits identify their corresponding data bits from the odd register of the "rb" register pair as write-enabled data bits. The instruction causes the write-enabled data bits to be written to a specified memory location. For this instruction, the memory location is specified by applying the immediate value (address offset) to the base address from the "ra" register. *See* '840 appendix, pp. 154-157; '599 appendix, pp. 128-130. The "S.MUX.64.B.A.I" instruction is precisely defined in full detail, down to the bit level, in a format that one of ordinary skill in the art would understand. A declaration from Mr. Korbin Van Dyke included with this Response further discusses the specific details of the "S.MUX.64.B.A.I" instruction as presented in the '840 appendix and '599 appendix.

Thus, the detailed description of the "S.MUX.64.B.A.I" found in the '840 appendix and '599 appendix provides proper support for the claimed invention. Specifically, the "S.MUX.64.B.A.I " instruction illustrates a specific example of a masked write operation using a mask "consisting of N independently selectable mask bits, N being an integer multiple of eight," as recited in claims 1 and 10, as well as a bit insertion operation using a second operand "consisting of N independently selectable bits, N being an integer multiple of eight," as recited in claims 19 and 26.

Written Description Requirement

The support found in the '840 appendix and '599 appendix clearly satisfies the written description requirement. To satisfy the written description requirement, a patent disclosure must describe the claimed invention in sufficient detail such that one of ordinary skill in the art can reasonably conclude that the inventor had possession of the claimed invention. MPEP § 2163(I). As discussed above, both the '840 and the '599 appendices describe the "S.MUX.64.B.A.I" instruction in full detail, down to the bit level. This instruction has been unambiguously defined,

as an illustrative embodiment of the invention. Other such instructions are disclosed as well. One of ordinary skill in the art would readily conclude upon reviewing the '840 and '599 appendices that Applicants had possession of the claimed invention. Further evidence that the '840 and '599 appendices satisfy the written description requirement is provided by way of a declaration from Mr. Korbin Van Dyke included with this Response.

Applicants respectfully disagree with the Office Action's rationale for rejecting the claims for lack of written description. The basis of this rejection is the contention that the mask bits of the instruction found in the disclosure supposedly cannot be independently selected "after the instruction is programmed." *See* Office Action, p. 2, last paragraph to p. 3, first paragraph ("This rejection assumes the scope of the claims provides for after the instruction is programmed the individually selecting each of the plural of fields or bits as write enabled or disabled") and p. 3, second paragraph ("These limitations are not described in the application as filed"). Applicants disagree with the Office Action's rationale for two important reasons, discussed below.

First, the claims do not recite any temporal limitations regarding when the mask bits must be "independently selectable." The Office Action states that the current rejection assumes the claims require that the mask bits must be "individually selectable" after the instruction is programmed. *See* Office Action, p. 2, last paragraph to p. 3, first paragraph ("This rejection assumes the scope of the claims provides for after the instruction is programmed the individually selecting each of the plural of fields or bits as write enabled or disabled") (*emphasis added*). However, there is absolutely no basis for making this assumption. The claims simply do not include such a temporal limitation. The claims require that the mask bits be "independently selectable," but they do not require that independent selection of the mask bits be performed

before the instruction is programmed, after the instruction is programmed, or at any other particular point in time.

Second, even if it is assumed that the claims include a temporal limitation requiring mask bits to be "independently selectable" after the instruction is programmed (which is not the case), the disclosure would still support such claims. This is because the "S.MUX.64.B.A.I" instruction defined in the '840 appendix and '599 appendix uses mask bits that are, in fact, "independently selectable" after the instruction is programmed. As discussed previously, the "S.MUX.64.B.A.I" instruction obtains its 64 mask bits from a specified register, the even register of the register pair specified by "rb." As one of ordinary skill in the art of computer programming would understand, use of a register such as the even register means that the contents of the even register can be modified as the computer program is being executed. In a typical example, as part of the execution of the computer program, the even register would be loaded with the independently selectable mask bits (*i.e.*, 1's and 0's) so the "S.MUX.64.B.A.I" instruction can be carried out properly. Clearly, such loading of the even register during execution of the computer program would occur well after the computer program (including the "S.MUX.64.B.A.I" instruction) is "programmed" or written by the computer programmer.

It appears that the Office Action may have concluded that the "S.MUX.64.B.A.I" instruction requires the mask bits to be supplied as an immediate value that is hard-coded at the time the instruction is "programmed" by the computer programmer.[2] However, this would be an incorrect conclusion. As discussed previously, the only operand of the "S.MUX.64.B.A.I" instruction that is specified as an immediate value is the address offset, which is used to specify

[2] For example, the Office Action states that "[t]he instructions disclosed in the instant application as originally filed provide for some mask fields or bits which provided as either write enabled and others write disabled but the particular mask bits that are enabled or disabled are not selectable. For a particular instruction the same mask bits are always selected as respectively enabled or disabled the way the instruction was originally programmed." *See* Office Action, p. 3, second paragraph.

the memory location to which write-enabled data bits are to be written. By contrast, the 64 mask bits used by the instruction are not specified as an immediate operand. Instead, the mask bits are obtained from the even register of the register pair specified by "rb." As discussed, the even register may be loaded with the appropriate mask during execution of the computer program, well after the programming of the computer program that includes the "S.MUX.64.B.A.I" instruction.

Thus, the '840 appendix and '599 appendix describe the claimed invention in sufficient detail to satisfy the written description requirement. The Office Action's position is based on an incorrect assumption that the claims include a temporal limitation requiring mask bits used by the instruction to be "independently selectable" after the instruction is programmed. However, the claims do not include such a temporal limitation. Furthermore, even if, for the sake of argument, it were assumed that the claims do include such a temporal limitation, the written description would still be satisfied, because the '840 and '599 appendices disclose an instruction whose mask bits actually are "independently selectable" after the instruction is programmed.

Enablement Requirement

The support found in the '840 appendix and '599 appendix also satisfies the enablement requirement. To satisfy the enablement requirement, a patent disclosure when filed must contain sufficient information regarding the subject matter of the claims as to enable one of ordinary skill in the pertinent art to make and use the claimed invention. MPEP § 2164.01. Whether the enablement requirement is met depends on whether undue experimentation would have been necessary for one of skill in the art to practice the invention in light of the disclosure. *Id.* As discussed above, the '840 and '599 appendices describe specific embodiments of an instruction for performing a mask write or bitwise insertion operation, including the "S.MUX.64.B.A.I"

instruction. The '840 and '599 appendices define this instruction in a manner that specifies the precise operation of the instruction, including exactly how every bit of data is obtained (*e.g.*, from specific registers, immediate values, memory locations etc.), operated on, and presented as output. One of ordinary skill in the art would not have been required to perform undue experimentation – or any experimentation at all for that matter – to understand exactly how the "S.MUX.64.B.A.I" instruction is carried out as an illustrative embodiment of the invention. As such, the '840 and '599 appendices clearly enable one of ordinary skill in the art to make and use the claimed invention. Further evidence that the '840 and '599 appendices satisfy the enablement requirement is provided by way of the declaration from Mr. Korbin Van Dyke included with this Response.

Applicants also respectfully disagree with the Office Action's rationale for rejecting the claims for lack of enablement. The Office Action contends that the mask of the disclosed instruction is fixed – *i.e.*, it cannot change. *See* Office Action, p. 4, first paragraph ("As disclosed the mask for each individual instruction cannot change"). This is simply not true. As discussed previously, the mask of the "S.MUX.64.B.A.I." is provided as an operand in the even register of the "rb" register pair. As one of ordinary skill in the art of computer programming would understand, use of a register such as the even register means that the contents of the even register can be modified as the computer program is being executed. Because the "S.MUX.64.B.A.I" instruction does not require the mask to be fixed or hard-coded, the mask can be changed without any of the "alteration of the instructions" or "mechanism to alter the instruction" suggested by the Office Action. *See id.* Instead, by obtaining the mask from a register, the even register of the "rb" register pair, the "S.MUX.64.B.A.I" instruction allows the mask to be changed during execution of the computer program, in a manner that one of ordinary

skill in the art would have been able to achieve, without any undue experimentation. For the reasons discussed above, Applicants submit that the support found in the '840 appendix and the '599 appendix satisfies the enablement requirement.

Non-obviousness of the Claims Under 35 U.S.C. § 103

In section 2 of the Office Action, claims 1-8 and 10-17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hao (U.S. Patent No. 4,569,016). In section 23 of the Office Action, claims 9 and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hao in view of Kabir (U.S. Patent No. 5,933,160). In section 26 of the Office Action, claims 19-23 and 26-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hao. In section 33 of the Office Action, claims 24, 25, 31, and 32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hao in view of Kabir. Applicants respectfully traverse.

Claims 1 and 10

Amended claims 1 and 10 each recite, *inter alia*:

> wherein in response to decoding a single instruction for writing data to memory based on a mask and data contained in at least one register, the mask consisting of N independently selectable mask bits, N being an integer multiple of eight, each of the mask bits corresponding to a data bit contained in the at least one register, each of the mask bits being independently selectable as either a write-enabled mask bit or a write-disabled mask bit . . . (*emphasis added*).

Claims 1 and 10 are both patentable over Hao. Hao fails to disclose the recited "writing data to memory based on a mask . . . consisting of N independently selectable mask bits, N being an integer multiple of eight." Hao's mask has either a three-part structure (*e.g.*, a substring of ones surrounded by zeros) or a two-part structure (*e.g.*, a substring of ones followed by zeros). *See* Hao at col. 26, lines 3-46. The bits of such a mask are not independently selectable as either

a write-enabled mask bits or write-disabled mask bit. For example, a three-part mask that is "a substring of ones surrounded by zeros" might appear as:

"00000000111111111111111111110000" (32-bit example)

The three-part structure of such a mask makes it impossible for the individual bits of the mask to be independently selectable. This is because all the bits in the "substring of ones" must have the same value (*i.e.*, "1"), so they cannot be independently selectable. In addition, all the bits outside the "substring of ones" also must have the same value (*i.e.*, "0"), so they too cannot be independently selectable. The same is true with respect to Hao's two-part mask. That is, all the bits in the "substring of ones" must have the same value (*i.e.*, "1"), so they cannot be independently selectable. In addition, all the bits that follow the "substring of ones" must have the same value (*i.e.*, "0"), so they too cannot be independently selectable. Thus, the structure of Hao's mask ensures that the mask does not "[consist] of N independently selectable mask bits, N being an integer multiple of eight," as recited in claims 1 and 10.

Even if Hao's mask is reconfigured, it still does not disclose the claimed invention. The Office Action points to a particular scenario in which Hao's mask is reconfigured by defining the "substring of ones" as a single bit, by choosing the rightmost index and the leftmost index of the substring to be the same bit position.[3] In such a scenario, all of the remaining bits outside this single bit must have the same value (*e.g.*, "0"). Clearly, these remaining bits outside the single-bit substring are not independently selectable – because they must all have the same value. Thus, even when reconfigured to have a single-bit substring, Hao's mask fails to "[consist] of N

[3] *See* Office Action at pp. 6-7, paragraph 5 ("Therefore the situation where the leftmost and rightmost indexes are the same is within the teachings of Hao. This situation would provide a selection of any single bit with the mask string individually depending on what same number the leftmost and rightmost indexes comprised. . . . Therefore The [sic] situation where the leftmost and rightmost indexes have the same value provide for a mask where Bit 21 indicates the value of an individually selected bit of the mask for selecting whether to enable or disable writing the corresponding single bit of the operand").

independently selectable mask bits, N being an integer multiple of eight," as recited in claims 1 and 10.

The Office Action also suggests that the mask can be reconfigured by changing the value of the substring and/or enlarging the size of the substring.[4] However, no matter how the value of the substring is changed and how the size of the substring is changed, Hao's mask is still limited to either a three-part structure or a two-part structure. It is impossible for these structures to produce a "mask consisting of N independently selectable mask bits, N being an integer multiple of eight," as recited. Thus, even if reconfigured to different combinations of substring values and substring sizes, Hao's mask would still fail to teach or suggest the claimed invention. For at least the reasons discussed above, claims 1 and 10 are patentable over Hao.

Claims 2-8 and 11-17

Claims 2-8 and 11-17 are rejected based on Hao. Claims 2-8 and 11-17 depend from and include all the limitations of claims 1 and 10, respectively. As such, dependent claims 2-8 and 11-17 are patentable over Hao, for at least the reasons stated above with respect to claims 1 and 10.

Claims 9 and 18

Claims 9 and 18 are rejected based on Hao in view of Kabir. Claims 9 and 18 depend from and incorporate all of the limitations of claims 1 and 10, respectively. As discussed above, Hao fails to disclose particular features of claims 1 and 10. Kabir fails to make up for the

[4] *See* Office Action at pp. 6-7, paragraph 5 ("Also Hao taught a system where any selected mask field (which can be one or more bits) can be enabled for write while the fields outside the mask can be select [sic] as enabled or disabled; or where the selected mask field can be disabled while the fields outside the mask field can be enabled or disabled. Note that each of these combinations are provided for as Hao taught all zeros or all ones zeros surrounded by ones or ones surrounded by ones where the size of the selectively masked field is selected using the boundary location bits (the situation where the bits surrounding the masked bit are the same condition of enabled or disabled are provided for by enlarging the mask field")

deficiencies of Hao with respect to these claimed features. As such, claims 9 and 18 are patentable for at least the reasons stated above with respect to claims 1 and 10.

Furthermore, claims 9 and 18 are patentable for the additional reason that Kabir fails to qualify as "prior art" against the present application. As discussed previously in this Amendment, the original disclosure of the present application provides proper support for the claimed invention to satisfy both the written disclosure and enablement requirements under 35 U.S.C. § 112. This establishes an effective filing date for the claimed subject matter of August 16, 1995. By contrast, the earliest possible effective filing date for Kabir is its actual filing date of November 27, 1995. Thus, Kabir does not qualify as prior art because its earliest effective filing date is later than the effective filing date of the present application.

For the reasons discussed above, claims 9 and 18 are patentable over Hao in view of Kabir.

Claims 19 and 26

Amended claims 19 and 26 each recite, *inter alia*:

> the execution unit capable of performing a bitwise insertion operation that operates on a first and a second operand stored in at least one register in the register file, the second operand consisting of N independently selectable bits, N being an integer multiple of eight, wherein each bit in the second operand is independently selectable as either having a first predetermined value or a second predetermined value . . . (*emphasis added*).

Claims 19 and 26 are both patentable over Hao. Hao fails to disclose "a bitwise insertion operation that operates on . . . [a] second operand consisting of N independently selectable bits, N being an integer multiple of eight," as recited. As discussed previously, Hao's mask has either a three-part structure (*e.g.*, a substring of ones surrounded by zeros) or a two-part structure (*e.g.*, a substring of ones followed by zeros). *See* Hao at col. 26, lines 3-46. The structure of Hao's

mask ensures that the mask does not "[consist] of N independently selectable bits, N being an integer multiple of eight," as recited in the claims.

Also, regardless of how Hao's mask is reconfigured, such as by defining the "substring of ones" as a single bit or changing the value and/or size of the "substring of ones," Hao's mask is still limited to either a three-part structure or a two-part structure. Much as discussed previously, it is impossible for these structures to produce an "operand consisting of N independently selectable bits, N being an integer multiple of eight," as recited. Thus, even if reconfigured to different combinations of substring values and substring sizes, Hao's mask would still fail to teach or suggest the claimed invention. For at least these reasons, claim 19 and 26 are patentable over Hao.

Claims 20-23 and 27-30

Claims 20-23 and 27-30 are rejected based on Hao. Claims 20-23 and 27-30 depend from and incorporate all the limitations of claims 19 and 26, respectively. As such, claims 20-23 and 27-30 are patentable over Hao, for at least the reasons stated above with respect to claims 19 and 26.

Claims 24, 25, 31 and 32

Claims 24, 25, 31 and 32 are rejected based on Hao in view of Kabir. Claims 24 and 25 depend from claim 19 and incorporate all of its limitations. Claims 31 and 32 depend from claim 26 and incorporate all of its limitations. As discussed above, Hao fails to disclose particular features of claims 19 and 26. Kabir fails to make up for the deficiencies of Hao with respect to these claimed features. As such, claims 24 and 25 are patentable for at least the reasons stated above with respect to claim 19, and claims 31 and 32 are patentable for at least the reasons stated above with respect to claim 26.

Furthermore, claims 24, 25, 31 and 32 are patentable for the additional reason that Kabir fails to qualify as "prior art" against the present application. As discussed previously, the original disclosure of the present application provides proper support for the claimed invention to satisfy both the written disclosure and enablement requirements under 35 U.S.C. § 112. This establishes an effective filing date for the claimed subject matter of August 16, 1995. By contrast, the earliest possible effective filing date for Kabir is its actual filing date of November 27, 1995. Thus, Kabir does not qualify as prior art because its earliest effective filing date is later than the effective filing date of the present application.

For at least the reasons discussed above, claims 24, 25, 31 and 32 are patentable over Hao in view of Kabir.

Conclusion

For at least the reasons discussed above, Applicants respectfully submit that the pending claims are not anticipated or rendered obvious by the cited art. Accordingly, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103.

Terminal Disclaimer for Overcoming the Double Patenting Rejection

On pages 17-30 of the Office Action, claims 1-32 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9 and 28-34 of copending Application No. 10/757,866. Applicants respectfully traverse.

As explained in MPEP 804.02(II), a terminal disclaimer may be filed to overcome a nonstatutory obviousness-type double patenting rejection. An appropriate terminal disclaimer under 37 C.F.R. § 1.321 is submitted with this Amendment to overcome the double patenting

rejection of claims 1-32. Accordingly, Applicants request withdrawal of the provisional rejection.

CONCLUSION

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If there are any outstanding issues that might be resolved by a telephone interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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